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Performance comparison of nanoscale double gate Ge and GaN finFETs

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Abstract
This paper presents a comparative study of the impact of Short Channel Effects (SCEs); threshold voltage variation, subthreshold swing and drain induced barrier lowering on both Ge and GaN FinFET devices. The analysis was carried out in the PADRE Simulator environment. The study also analyzes the transconductance and drive currents of these materials. The results reveal that the use of Ge as a channel material for FinFET devices can result in higher drive currents and transconductance compared to GaN-based devices. However, Ge-FinFETs are more prone to short channel effects, which can impact their performance. On the other hand, GaN-based FinFETs show better immunity to short channel effects, but their transconductance and drive currents are comparatively lower. This finding contributes valuable insights that can significantly advance the development and optimization of FinFET devices employing Germanium and Gallium Nitride as channel materials.

Keywords: Channel material, Drive currents, DIBL, SCEs, Transconductance

1. Introduction

The field of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology is currently undergoing a significant shift in the materials and device architectures used to improve performance and scalability. With the planar bulk Silicon MOSFET reaching its scaling limit, researchers are exploring new materials and device designs to enhance performance [1]. However, the scaling down to the nanometer range has resulted in the emergence of short channel effects, which can negatively impact the system's performance and reliability [2]. This has led to the development of the FinFET, a device architecture that can effectively control short channel effects (SCEs) and exhibit minimal variability[3].

In order to improve the performance of the FinFET, researchers are investigating the use of compound semiconductors such as Gallium Nitride (GaN), Gallium Arsenide (GaAs), and Gallium Antimonide (GaSb) as channel materials, replacing the conventional silicon and germanium [4]. Nevertheless, the potential benefits of improved performance and scalability make the exploration of these new materials and device designs an exciting area of research in the field of nanoelectronics.

The utilization of certain compound semiconductors in lieu of traditional silicon as channel materials in FinFET devices has been reported in literature. In a bid to obtain a channel material with reduced short channel effects, an Investigation of nanoscale double-gate n-FinFETs with different channel materials and gate dielectrics was carried out [5]. The study utilized SiGe and 3C-SiC materials in the channel region and employed the numerical simulation tool (Atlas Silvaco) to evaluate the electrical characteristics of the device at 300K. The authors demonstrated that using SiGe as the channel material leads to higher drain current and transconductance. A study conducted to compare different channel materials such as Silicon (Si), Gallium Arsenide (GaAs), Indium Arsenide (InAs), Indium Phosphide (InP), and Indium Antimonide (InSb) by Prasher et al. [4] showed that InSb outperformed the other materials when used in MOSFET devices. This is due to its higher on-current and transconductance, as well as its ability to mitigate short channel effects. In a comparison between Ge, Si, and GaAs by Shafiqul et al. [1], GaAs emerged as the optimal channel material for FinFET devices due to its superior performance in mitigating short channel effects in comparison to Ge and Si.

Another research was carried out to investigate the short channel effects in Si, GaAs, GaN, and GaSb [6]. The results of the research showed that GaN exhibited the poorest performance among the channel materials. The impact of downscaling the nano-channel dimensions of Indium Arsenide Fin Field Effect Transistor (InAs-FinFET) on its electrical characteristics was studied by Mahmood et al. [7]. The authors investigated the ION/IOFF ratio, Subthreshold Swing, Threshold voltage and Drain-induced barrier lowering of the transistor based on variable channel dimensions: length, width, and oxide thickness. The authors concluded that the InAs-FinFET performed best with a channel length of 25 nm, providing a high ION/IOFF ratio and a subthreshold

swing value close to the ideal one. In another research conducted by Jena et al. [3], Si and GaN were compared at different biasing conditions to determine the better channel material that can be used in FinFET devices. GaN was found to have superior performance to Si. However, there is limited investigation into the short channel effects under diverse biasing conditions using Germanium and Gallium Nitride as channel materials.

The aim of this research paper is to investigate how short channel effects impact FinFET devices that utilize Ge and GaN as channel materials at different biasing conditions. Additionally, a comparison of the results obtained from both materials were presented. The paper also presents the findings regarding the transconductance and drive currents of these materials.

2. Materials and method

2.1 Device structure

Figure 2.1 depicts the device structure of a double gate n-channel FinFET. The structure includes essential components such as the source, drain, gate length (also known as channel length), and channel width (referred to as fin width or fin thickness). In the case of a triple gate FinFET, an additional top gate is activated by utilizing an extremely thin top oxide layer. The oxide is positioned on both sides of the fin's side walls and, on the fin's, top surface before establishing the gate contact. The thickness of the side wall oxide is denoted as tox1 and tox2 [6].

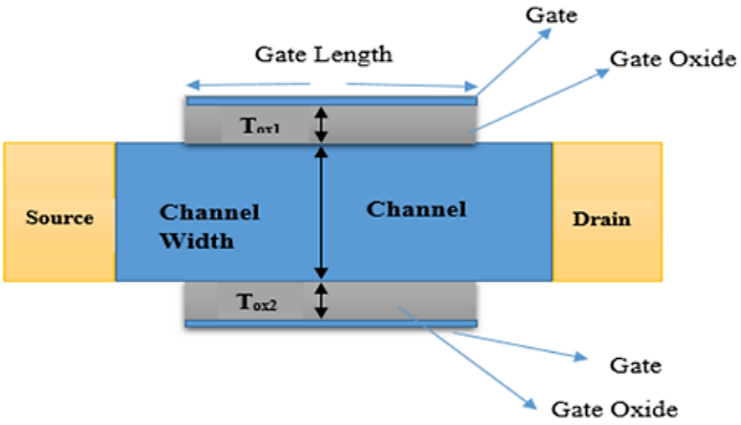

Figure 2.1: Device structure

2.2 Simulation tool

The proposed device was simulated using a noteworthy PADRE Simulator from MuGFET tool available on nanoHUB.org as part of this research study. Purdue University (USA) developed and designed the MuGFET tool, which can run simulations using either PADRE or PROPHET. Bell Laboratories invented both PADRE and PROPHET. PROPHET is a profiler for partial differential equations that can be applied to one, two, or three dimensions, while PADRE is a simulator for 2D or 3D devices of any shape. The software can produce useful FET curves, which are particularly helpful for engineers in explaining the fundamental physics of FETs. In addition, it can provide self-consistent solutions for poison and drift-diffusion equations [1, 8].

2.3 Simulation parameters

Using Ge and GaN as channel materials, the simulation tool examines the characteristics of FinFET by analyzing the output characteristic curves of the transistor. Table 2.1 provides a list of simulation parameters used to evaluate the device at a temperature of 300K.

Table 2.1: Simulation parameters

Parameter	Value
Gate Length	45nm
Channel width	10nm
Oxide thickness 1	2nm
Oxide thickness 2	2nm
Initial gate bias	0V
Final gate bias	1V
Initial drain bias	0.05V
Final drain bias	1V
Source extension length	50nm
Drain extension length	50nm
Band gap for GaSb	3.5 Ev
Electron mobility for GaSb	1000 cm2/V-S
Hole mobility for GaSb	200cm2/V-S
Electron affinity for GaSb	4.10eV

3. Results and Discussion

Various figures were used in this paper to compare the results of Ge and GaN FinFETs. The transconductance, on-current, threshold voltage, subthreshold swing, and drain induced barrier lowering of both materials were plotted and analyzed. The results were obtained at various values of drain and gate voltages.

3.1 Drain current variation with gate voltage

Figure 3.1 presents a graph plotting the drain currents of Ge-FinFET and GaSb-FinFET for varying gate voltages. The study was carried out at a fixed channel width of 10nm, the oxide thickness of 2nm and the gate length was kept at 45nm. It can be observed that Ge-FinFET presents highest on-current of about 1.38×10^{-4} A/μm at a gate voltage of 1V in comparison with GaN-FinFET. This is due to the fact that Ge has higher mobility than GaN.

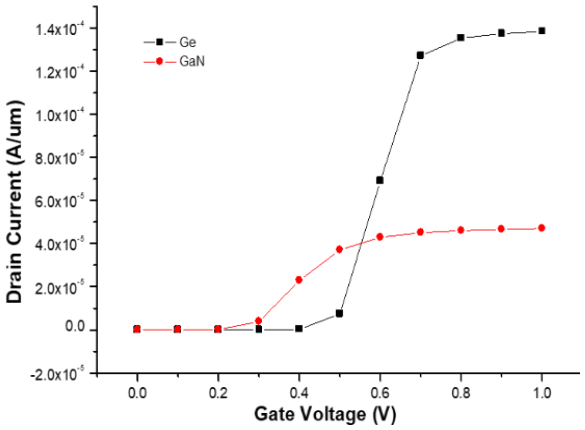

Figure 3.1: Drain current Vs Gate voltage

3.2 Transconductance variation with drain voltage

The transconductance, denoted as gm, is a critical parameter that provides a quantitative measure of how the drain current (ID) changes in response to variations in the gate-source voltage (VGS) while maintaining the drain-source voltage (VDS) at a constant value [7-9]:

$$g_m = \frac{dI_D}{dV_{GS}} \qquad (1)$$

where V_{GS} is gate-source voltage and I_{DS} is the drain-source voltage.

It essentially describes the sensitivity or efficiency of the transistor in modulating its output current in response to changes in the input voltage applied to the gate terminal, and this is a fundamental characteristic in the analysis and design of field-effect transistors. Figure 3.2 presents the comparison of transconductance of Ge-FinFET and GaN-FinFET which was conducted at constant 10nm channel width, 45nm gate length and oxide thickness of 2nm. It is clear from this that transconductance in Ge-FinFET increases as the drain voltage increases from 0.35V to 0.55V. Ge demonstrate highest transconductance of about $6.17 \times 10^{-4}\ S/\mu m$ at a drain voltage of 0.55V.

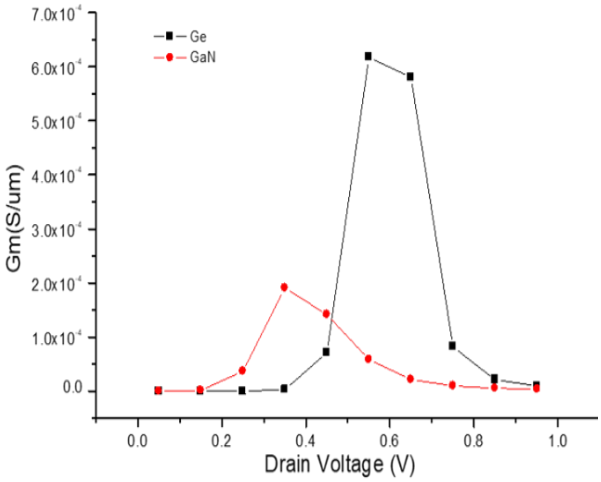

Figure 3.2: Transconductance Vs Drain voltage

3.3 Threshold Voltage Variation with Drain Voltage

The Threshold voltage is the minimum gate voltage required to set up a conduction path between the source and the drain. The threshold voltage expression in case of a multi-gate field effect transistor (MuGFET) device structure can be expressed according to Mustafa et al. [9] as:

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \qquad (2)$$

where Q_{SS} represents charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, f_{ms} represents metal semiconductor work function difference between gate electrode and the semiconductor, f_f is the fermi potential, and Vin is the additional surface potential to $2f_f$ that is needed for ultrathin body devices to bring enough inversion charges in to the channel region of the transistor to reach threshold point.

Figure 3.3 presents the comparison of threshold voltage variation of Ge-FinFET and GaN-FinFET. For this work, the channel width, which is kept constant at 10nm, while as the oxide thickness was kept fixed at 2 nm and the gate length was kept at 45nm. The threshold voltage decreases with increase in the drain voltage. It was observed that, the GaN-FinFET presents lowest threshold voltage of 0.48V at a drain voltage of 1V compared to the Ge-FinFET. This characteristic gives GaN-FinFET an advantage in terms of faster switching operation. This same behavior was reported in the work of Jena *et al.* [3].

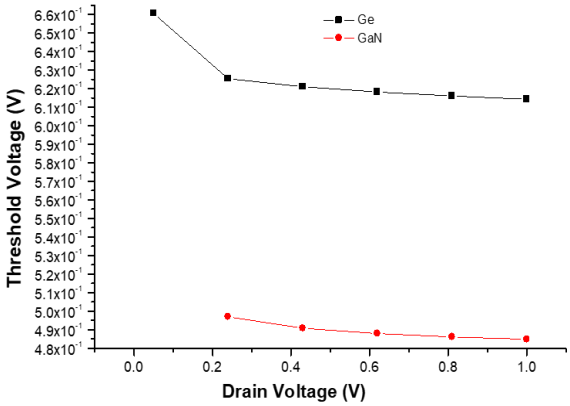

Figure 3.3. Threshold Voltage Vs Drain Voltage

3.4 Subthreshold swing variation with drain voltage

The key factor in determining the leakage current is the subthreshold slope. Moreover, the calculation of SS is performed using equation 3 [8]:

$$SS\ (mV/\ dec) = \frac{d\ V_{GS}}{d\ (log_{10}\ I_{DS}} \qquad (3)$$

where V_{Gs} is the gate-source voltage and I_{DS} is the drain-source current.

The comparison between the subthreshold swings of GaN-FinFET and Ge-FinFET presented in Figure 3.4 clearly demonstrates that, the subthreshold swing of GaN-FinFET decreases as the drain voltage increases. Also, it was observed that, the GaN-FinFET presents lowest SS value of 65.28mV/dec at 0.05V as compared to Ge-FinFET. This characteristic is crucial for achieving efficient operation in a FinFET device. A common SS parameter for a MuGFET is 60mV/decade, indicating that a 60mV alteration in gate voltage results in a tenfold variation in drain current [5].

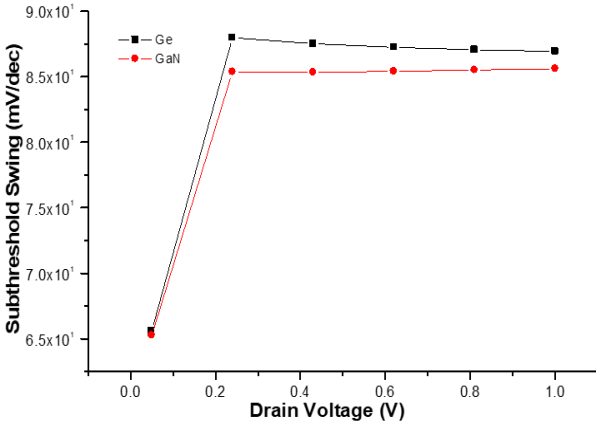

Figure 3.4: Subthreshold swing Vs drain voltage

3.5 Drain induced barrier lowering variation with drain voltage

Drain Induced Barrier Lowering is defined as the decrease in the threshold voltage when the drain voltage is increased from low to high value [10]. Drain Induced Barrier Lowering can be calculated using equation [4]:

$$DIBL\left(\frac{mV}{V}\right) = \frac{\Delta\ V_{TH}}{\Delta\ V_{DS}} \qquad (4)$$

where V_{TH} is the threshold voltage and V_{DS} is the drain-source voltage.

Figure 3.5 illustrates a comparative analysis of GaN-FinFET and Ge-FinFET devices concerning drain induced barrier lowering which one of the Short Channel Effects (SCEs) is observed in FinFET devices. The obtained results demonstrate that GaN-FinFET showcases the lowest drain induced barrier lowering value of 6.97mV/V at a drain voltage of 1V when compared to Ge-FinFET. This characteristic is crucial for achieving high efficiency in a FinFET device. This agrees with the findings reported in Hadri and Patanè [5].

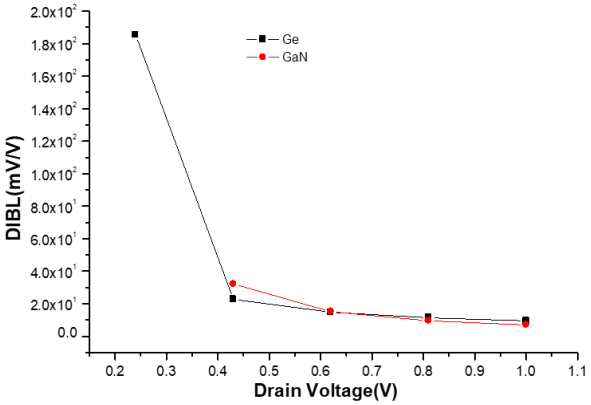

Figure 3.5: DIBL variation with drain voltage

Table 3.1: Summary of the main findings for Ge and GaN-FinFETs in comparison with ITRS 2013[2]

Characteristics	Ge-FinFET	GaN-FinFET	ITRS 2013
Ion (A/μm)	1.38×10^{-4}	4.70×10^{-5}	
Ioff (A/μm)	9.43×10^{-13}	9.46×10^{-11}	
$\frac{I_{on}}{I_{off}}$	1.46×10^{9}	4.97×10^{5}	
Gm (S/μm)	6.17×10^{-4}	1.91×10^{-4}	
Vth (V)	0.62	0.48	0.461±12.7%
SS (mV/dec)	65.62	65.28	70-90
DIBL (mV/V)	9.39	6.97	

4. Conclusions

The comparative study conducted on the impact of short channel effects on Ge and GaN-FinFET devices revealed that Ge-based FinFETs can offer higher drive currents and transconductance than the GaN-based FinFETs. However, they are more susceptible to short channel effects which can negatively affect their performance. In contrast, GaN-based devices have better immunity to short channel effects but exhibit comparatively lower transconductance and drive currents. The results obtained from this study offer valuable insights that can be utilized to develop and optimize FinFET devices using Ge and GaN as channel materials. Further research can be done to investigate the possibility of combining Ge and GaN materials in a single FinFET device so as to leverage the advantages of both materials. This may involves exploring other ways of optimizing the material interfaces, doping profiles or device architectures to achieve improved performance characteristics, such as higher drive currents, better immunity to short channel effects and enhanced transconductance.

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