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LINE OUTAGE CONTINGENCY ANALYSIS INCLUDING THE SYSTEM ISLANDING SCENARIO

A. Amin Eskandari Dehkordi[1,*] and B. Hasan Meyar Naimi[2]

[1]Department of Electrical Engineering, Payam-University of Applied Science and Technology, Shahr-e Kord, Iran

[2]Department of Electrical Engineering, Isalamic Azad University of Hamedan, Hamedan, Iran

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ABSTRACT

The paper describes an algorithm for determining the line outage contingency of a line taking into account of line over load effect in remaining lines and subsequent tripping of over loaded line(s) leading to possible system split or islanding of a power system. The optimally ordered sparse [B'], [B''] matrices for the integrated system are used for load flow analysis to determine modified values of voltage phase angles [d] and bus voltages [V] to determine the over loading effect on the remaining lines due to outage of a selected line outage contingency. In case of over loading in remaining line(s), the over loaded lines are removed from the system and a topology processor is used to find the islands. A fast decoupled load flow (FDLF) analysis is carried out for finding out the system variables for the islanded (or single island) system by incorporating appropriate modification in the [B'] and [B''] matrices of the integrated system.

Keywords: Contingency; Line outage; Rotating mass; System islanding.

Author Correspondence, e-mail: am.eskandari256@gmail.com

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1. INTRODUCTION

Line outage contingency indices provide a measure of the overall effect on the system due to that line outage. Line outage contingency indices for a power system based on its operating conditions indicate the relative severity of the line outage contingency for the system operation. These help operator to take some corrective/preventive measure so as to prevent large system disturbances (over loading of lines) leading to cascade tripping and system collapse. Ejebe and Wollenberg [1] have reported a pioneering work in which they have formulated a method of contingency ranking based on system performance indices (PI) which are functions of bus voltages and line flows and the corresponding limits. This method also uses Tellegen's theorem to calculate PI sensitivities to these outages. The ranking is done by ordering these PI sensitivities in descending order. Irissari and Leven [2] have proposed a method for contingency ranking based on DC load flow, which is computationally less complex. Mikolinnas and Wollenberg [3] have presented an improved version of the Megawatt PIs by including all terms in the infinite Taylor's series expansion for all the change in the performance index due to different outage. Irissari and Sasson [4] have proposed an improved computational procedure based on DC load flow method, which requires one forward– backward substitution to compute performance index for line outage. Vemuri and Usher [5] have presented a unified approach to find sensitivity of performance index for single branch outage, generation/load outage and combination of them.

Most of the literature on contingency ranking based on analytical methods show that ranking by PI methods are widely accepted [6]. The megawatt performance index, PI_{MW} is used as an index for quantifying the extent of line overloads in terms of megawatt flows and their MW limits. However, megavoltampere performance index PI_{MVA} quantifies the line over load in terms of magavoltampere flows and their MVA limits. It has been reported that PI_{MVA} represents extent of line over load in true sense as MVA flow in a line corresponds to the line current in that line [1].

In certain cases outage of a line may split system into two islands or due to outage of a line, over load may appear in remaining line(s) and overloaded lines may trip leading to system split. Immediately after split, a power balance between generation, load and losses for each

island must take place. Since, the power drawn by the loads do not change instantaneously, the imbalance in power is supplied/absorbed by the generators affecting a change in the kinetic energy (KE) of its rotating mass. Thus, change in electrical output of each generator in the island will be proportional to the KE of its rotating mass, i.e. its inertia (H). Therefore, in order to simulate the condition immediately after a system split, rescheduling of generation for the power balance in islands have to be done before a load flow can be carried out to obtain the line flows after islanding. Under such situation only PI_{MVA} may not reflect the overall effect on the system due to that line outage. The system voltage conditions are also taken into account to quantify the effect on the system due to that line outage. As such, voltage stability index is used to examine system voltage stability condition.

In this paper, PI_{MVA} along with voltage stability index are determined to quantify the line outage contingency of a power system. For this purpose, optimally ordered sparse [B'], [B''] Matrices are used to determine voltage phase angles [δ] and bus voltages [V] for a line outage applying appropriate modifications of [B'], [B''] and Y-bus matrices. Then using these modified [V] and [δ] line flows for the remaining lines are computed, if any line over loading in line(s) are detected among the remaining lines, the over loaded lines are removed from the network and a topology processor is used to determine possible system islanding. When a system split is detected (indicated by c value or by the topology processor), appropriate modifications are carried out on the sparse [B'] and [B''] matrices depending upon the change in network configuration. A slack bus is allocated for each island. For this a high value is placed at the diagonal element of [B'] and [B''] matrices corresponding to that bus location. No change in matrix storage and ordering for sparse [B'] and [B''] is required. In order to obtain a balance between generation, demand and loss in each island immediately following a system split, generation rescheduling is carried out by finding the change in generation for each generator based on its inertia and the total change in power required for power balance in the island. A load flow using the sparse and ordered [B'] and [B''] matrices is carried out to determine the state of the islands and line flows are computed. Based on the system operating condition line outage contingency indices are computed.

2. FAST DECOUPLED LOAD FLOW ANALYSIS FOR ISLANDED SYSTEM

In a fast decoupled load flow analysis the solution matrix, [B'] and [B''] matrices remain unchanged during load flow analysis [7]. Therefore, ordering and factorization for each of them are done once at the beginning only in a load flow program. In a power system a slack bus is required to take care of system real and reactive losses. For the slack bus voltage magnitude (V) and voltage phase angle (d) are known variables and so do not change during load flow iterations. Therefore, row and column of [B'] matrix corresponding to slack bus are not included while forming [B'] matrix in fast decoupled load flow analysis. The same effect can be achieved by using [B'] matrix having row and column corresponding to slack bus included but with a large (10^6) value in place of the diagonal element in [B'] matrix. Without loss of generality taking bus number 1 as the slack bus, the change in real power injection at bus bars can be expressed as:

$$\begin{bmatrix} \Delta P_1 / V_1 \\ \Delta P_2 / V_2 \\ \dots \\ \Delta P_N / \Delta V_N \end{bmatrix} = \begin{bmatrix} 10^6 & B'_{12} \dots B'_{1N} \\ B'_{21} & B'_{22} \dots B'_{2N} \\ \vdots & \\ B'_{N1} & B'_{N2} \dots B'_{NN} \end{bmatrix} \begin{bmatrix} \Delta\delta_1 \\ \Delta\delta_2 \\ \vdots \\ \Delta\delta_N \end{bmatrix} \quad (1)$$

Large value in place of diagonal element corresponding to slack bus allow no change in voltage phase angle (i.e. $\Delta\delta_1$ is very insignificant) for that bus while solving the above equations for [$\Delta\delta$]. Thus, the bus assigned as slack bus for an island will retain the required characteristic of a slack bus of a power system(where di and Vi are defined variables) and ΔP Vi/Δ Vi for the slack bus for an island is to be assigned as zero. The islanded system is the subsystems of the main grid system, therefore, the factored [B'] and [B''] matrices used for the load flow analysis of the grid system can be used for the islanded system with the following modifications:

1. For outage of line ij, [B'] matrix is modified by placing zero at positions ij and ji and subtracting B′ij from B′ii and B′jj in [B'] matrix. Similar modifications are made in [B''] matrix.

2. For each island a slack bus is required. For this purpose, in each island a generating bus with sufficient generation reserve and voltage phase angle close to the mean value of voltage

phase angle for all the buses in the island is selected as a slack bus. This choice of slack bus results in faster convergence as maximum voltage angle difference (δij) between buses in each island remains small thus complying with the FDLF method assumptions. Slack bus being the reference for voltage phase angle, it's voltage magnitude and voltage phase angle must remain unchanged during load flow analysis. To achieve this, large (10^6) values are put in place of the diagonal elements corresponding to the slack buses of the islands of [B'] and [B''] matrices of the integrated system, which is already stored in ordered form. Now, reduction of [B'] and [B″] matrices are carried out.

3. As the system get separated into number of islands, at the instant of bifurcation for each island generation—demand balance is obtained by modifying the generation in the island to balance the load in that island. This change in generation is calculated based on the relative inertia of the machines as follows:

Generation from each generator of an island are calculated as follows

$$P_{gij} = P_{Gj} + \frac{(P_{gti} - P_{GTi}) H_j}{\sum_{j=1}^{N_i} H_j} \quad (2)$$

where

N_i total number of generator in ith island

P_{Gj} generation from jth generator before system bifurcation

H_j inertia constant of jth generator in ith island

P_{gij} generation from jth generator in ith island after the system bifurcation

P_{GTi} total generation from the generators located in ith island at the time of system bifurcation

$P_{gti} = P_{dti} + P_{li}$

P_{gti} required total system generation for ith island

$$P_{li} = \frac{P_L P_{dti}}{P_{DT}}$$

where

P_L total system loss for the system before bifurcation

P_{li} expected system loss for ith island

P_{DT} total system demand before system bifurcation

*P*dt*i* total system demand for *i*th island.

Let us take a case of system bifurcation, which results in formation of two islands. Now, selecting bus 1 and bus *m* as the slack buses for the two islands, respectively, the fast decouple representation of [*B*′] matrix relating [δ] and [Δ*P*] is as follows:

$$\begin{bmatrix} \Delta P_1/\Delta V_1 \\ \Delta P_2/\Delta V_2 \\ \Delta P_3/\Delta V_3 \\ \Delta P_4/\Delta V_4 \\ \vdots \\ \Delta P_m/V_m \\ \Delta P_{m+1}/V_{m+1} \\ \Delta P_{m+2}/V_{m+2} \\ \Delta P_{m+3}/V_{m+3} \\ \Delta P_{m+4}/V_{m+4} \\ .... \\ \Delta P_N/V_N \end{bmatrix} = \begin{bmatrix} 10^6 & B'_{12} & \cdots & 0 & \cdots & B'_{1N} \\ B'_{21} & B'_{22} & \cdots & & \cdots & B'_{2N} \\ B'_{31} & B'_{32} & \cdots & 0 & \cdots & B'_{3N} \\ B'_{41} & B'_{42} & \cdots & 0 & \cdots & B'_{4N} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 10^6 & \cdots & B'_{mN} \\ B'_{(m+1)1} & B'_{(m+1)2} & \cdots & 0 & \cdots & B'_{(m+1)N} \\ 0 & 0 & \cdots & B'_{(m+2)m} & \cdots & B'_{(m+2)N} \\ 0 & 0 & \cdots & B'_{(m+3)m} & \cdots & B'_{(m+3)N} \\ 0 & 0 & \cdots & B'_{(m+4)m} & \cdots & B'_{(m+4)N} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ B'_{N1} & B'_{N2} & . & 0 & . & B'_{NN} \end{bmatrix} \begin{bmatrix} \Delta\delta_1 \\ \Delta\delta_2 \\ \Delta\delta_3 \\ \Delta\delta_4 \\ \vdots \\ \Delta\delta_m \\ \Delta\delta_{m+1} \\ \Delta\delta_{m+2} \\ \Delta\delta_{m+3} \\ \Delta\delta_{m+4} \\ \vdots \\ \Delta\delta_N \end{bmatrix} \quad (3)$$

The details about the modifications to be carried on [*B*′] matrix of integrated system in case of system islanding are explained in Appendix A with the help of a sample six bus system. Introduction of above-mentioned steps provides the following advantages:

1. Separate calculation and storage of [*B*′] and [B″] matrices for individual island are avoided.

2. As the modification of [*B*′] and [*B*″] matrices are carried out on the matrices, which are already ordered, it saves considerable CPU time.

3. NETWORK TOPOLOGY PROCESSOR

Network topology defines the connectivity of power system devices among each other.

A power system network is configured to satisfy system operation. Power system network connectivity does not remain static because it’s devices change their status (ON/OFF) from time to time due to various reasons. Normally, a change in network topology is characterized by the change in status of transmission line(s) from ‘ON’ to ‘OFF’ state or from ‘OFF’ to ‘ON’

state. System disturbances like fault, sudden line overload, etc. may lead to tripping of transmission line(s) to stop propagation of the disturbance to the healthy portion of the network. Changes in topology of a network may sometime lead to system bifurcation resulting in creation of islands. Under such situation, it is essential to determine network topology of each island to carry out load flow of the islanded system. In addition to this, power system operation/planning requires modification of network configuration to ascertain the probable impact of the change in the performance of the system. One such important analysis is line outage contingency analysis of a power system. During line outage contingency analysis, some times network split (bifurcation) occurs due to outage of line(s). This creates independent islands in the integrated system. To determine the effect of such line outage, one has to carry out load flow for the islanded system. This is possible only after knowing the network topology of the islanded system. Therefore, a network topology processor is required to determine the topology of the system.

A conventional topology processor examines the connectivity among the nodes (buses) of a power system and based on this analysis, it determines topology of the system network. It, basically, aims at determining the followings:

1. System island(s) (in case of system bifurcations/islandings, number of islands (NIS) is always more than one).
2. Status of the island(s) (SI) (Active island (IS_k=1), i.e. island has both load and generation and Dead Island (IS_k=0), i.e. island has only load (s) or only generation (s)).
3. Buses in each island (BI_k) and lines in each island (LI_k).
4. Index k represents island number

An active island has both loads and generations, therefore, there are power flow in the lines. Whereas, a dead island does not have any active source (generator) in it and therefore, this island is not energized (blackout). Under normal operating condition of an integrated power system the topology processor indicates the system as one island. During emergency and restorative mode of power system planning/operation, the network topology keeps changing. Thus, power system planning/operation under such condition requires continuous checking of network topology after every switching of network elements (line/transformer). Therefore, a

network topology processor constitutes an integral part of a power system analysis during emergency and restorative mode of planning/operation.

Network topology processor uses the status of lines (i.e. ‘ON’ or ‘OFF’) to determine the connectivity among the buses in a power system. This aims at listing bus numbers and line numbers in an island until the continuity is broken. Therefore, it is essential to organize the search process in a proper way so as to avoid unnecessary repetition of the search steps. To achieve this objective the following strategy is used in the proposed topology processor:

1. A compact data structure (bus data structure) is created showing the line number connected to each bus of the system. This structure is exploited extensively to check the connectivity among the nodes during search process.

2. Once a bus or a line undergoes the search process, it is given ‘included status’ (i.e. the bus or the line is included in the island under process) and for the rest of the search process they are not considered.

3.1. Creation of bus data structure

A row vector ‘LINB’ is used to store the number of lines connected to each bus. This vector is determined at the time of reading the line data. The line data is associated with ‘from bus’ number (vector ‘SB’) and ‘to bus’ number (vector ‘EB’). The dimensions of the vectors ‘LINB’, ‘SB’ and ‘EB’ are 1×N, 1×NL and 1×NL, respectively. Based on the row vector ‘LINB’, another row vector ‘SLOCB’ (1×N) is created to store the starting serial number of a row vector ‘LNOB’ which contains line numbers corresponding to each bus. Since, each line appears with two end buses, the size of ‘LNOB’ is 1×2NL. The schematic diagram of the storage scheme is shown in Fig. 1. For ith bus, the starting location of line elements connected to this bus (n) is stored in SLOCBi and total lines connected (m) to this bus is stored in LINBi. Storing of line numbers in the row vector ‘LNOB’ has to be done through a search process. To complete this task only in one search for all lines, another ‘POINT’ (1×N) is used. Initially, ‘POINT’ points the starting location of ‘LNOB’ for each bus. While storing line numbers for each bus, ‘LNOB’ offers entry location to ‘LNOB’ depending upon bus numbers (i.e. ‘SB’ and ‘EB’) associated with each line and for the two buses ‘POINT’ are incremented by one. Thus, for each line ‘LNOB’ gets two entries. Once ‘LNOB’, ‘SLOCB’ and ‘LINB’ are stored for any

bus, the line connected to this can be obtained directly from this ‘Bus Data Structure’.

This arrangement allows quick search for connectivity between buses, which are connected.

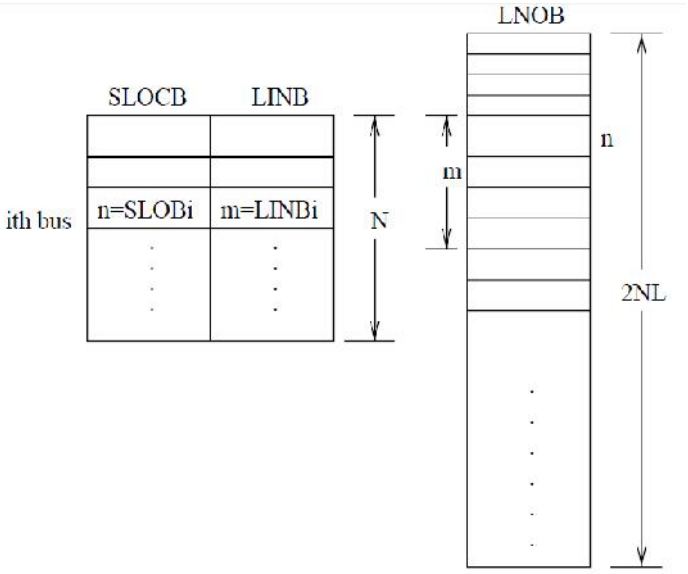

Fig.1. The schematic diagram of the storage scheme of line numbers connected to each bus

3.2. Basis for the search procedure

Two row vectors ‘BINCL’ (1×N) and ‘LINCL’ (1×NL) are used to store island number indicating the buses and lines in the respective islands. These two vectors are initialized to ‘zero’ before beginning the search operation. Another vector ‘LUP’ (1×N) is used to keep count of lines already searched for each bus. This vector is also initialized to ‘zero’ before beginning the search operation. The use of ‘LUP’ reduces number of line to be checked as, starting line number of a bus picked up for search process is given by $k = SLOB_i + LUP_i$.

The search process begins setting island counter as 1 (i.e. first island; ISNO=1), first bus of ‘bus data file’ is taken as the first bus (SBUS) of this island and ‘$BINCL_1$’ is made 1 to provide ‘included status’ which indicates that this bus in included in first island. The search is done from this bus to the next bus (NBUS) connected by the first line of ‘Bus Data Structure’ corresponding to this bus and ‘BINCL’ and ‘LINCL’ are provided with ‘included status’ with the island number. Thus, from bus to bus searches are carried out using ‘Bus Data Structure’ to select the next line for search. During each entry to ‘Bus Data Structure’, if line status (LSAT) is found with status ‘ON’ and ‘LINCL’ is found ‘zero’ (i.e. does not under go search process) then ‘to end bus’ (EB) of that line is taken as the next bus (NBUS) to continue with

the search process. Flag FLAG1 is used to indicate the continuity of search process. This flag is initialized to ‘zero’ for each entry of search operation. The status of this flag is made ‘one’ when continuity to the next bus is found. Once this continuity is broken, search is made in ‘bus data file’ to check whether any bus with ‘included status’ has line having ‘zero’ value in ‘LINCL’ (i.e. this line does not under go search process). For this purpose flag FLAG2 is used. If such condition is encountered, this flag is set to ‘one’ and ‘to end bus’ (EB) of that line is taken as (NBUS) to continue with the search process. If during the search process FLAG1 and FLAG2 become ‘zero’, this indicates that for the current island all buses and lines are searched and included in ‘BINCL’ and ‘LINCL’, respectively. Now, at this stage another check is made to determine whether ‘BINCL’ has any ‘zero’ value. This indicates that system has more than one island. For this purpose, flag FLAG3 is introduced. This flag is set to ‘zero’ and ‘BINCL’ is checked from beginning to determine the location of ‘BINCL’ which has ‘zero’ value. If such situation exists, FLAG3 is made ‘one’ and this location corresponds to the bus number to be taken as the first bus (SBUS) for the search process for the next island. Therefore, island counter is increased (ISNOZISNOC1) and search process of the next island is carried out. Finally, when all buses and lines attain ‘included status’ in ‘BINCL’ and ‘LINCL’, then all three flags become ‘zero’. This indicates the end of search process. After this, for all islands, loads and generations are checked, an island with active generation(s) and load(s) is provided with active status (‘ON’) and an island without active load and generation is provided with dead status (‘OFF’). Finally, for each island a slack is determined using the basis described in Section 2. The details about each step of the topology processor are shown in the flow chart given in Fig. 2

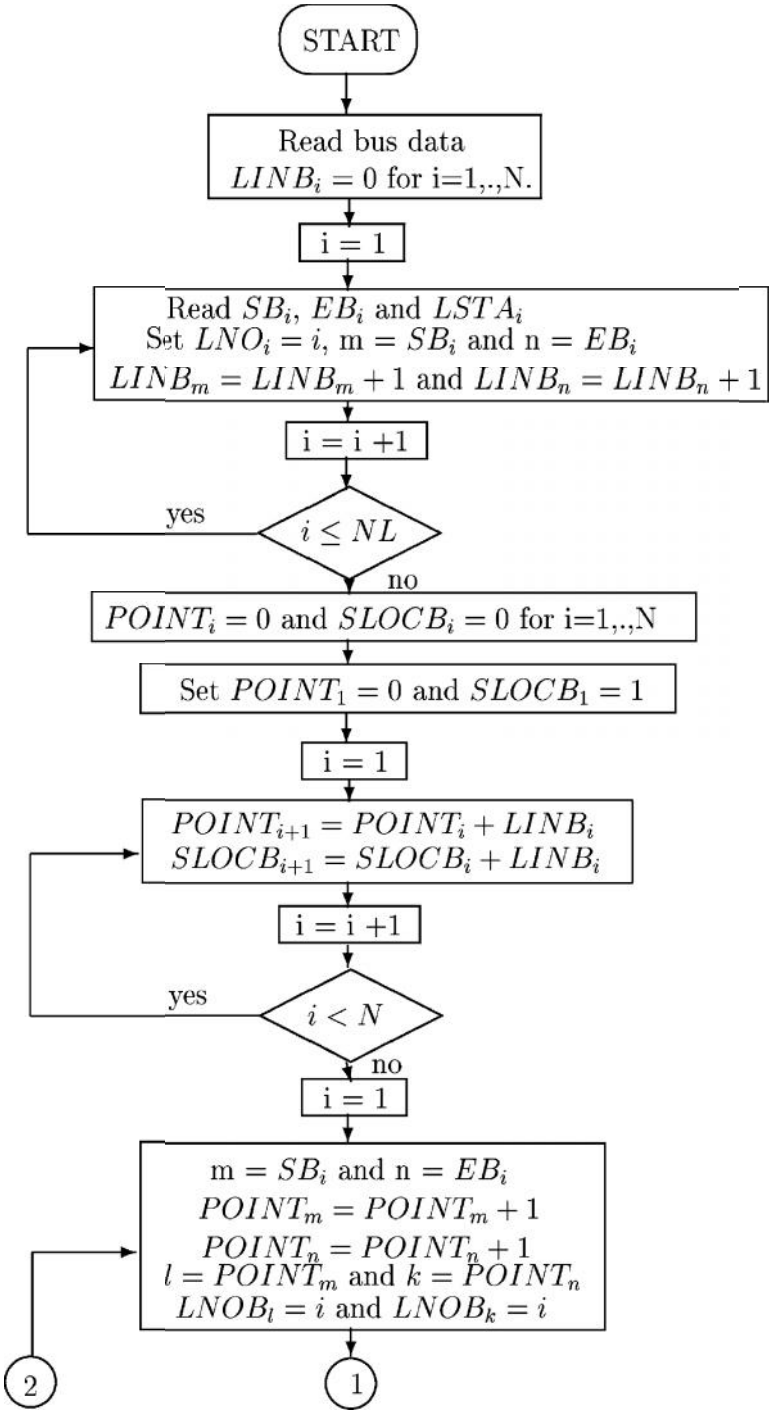

Fig.2. Flow chart for the topology processor

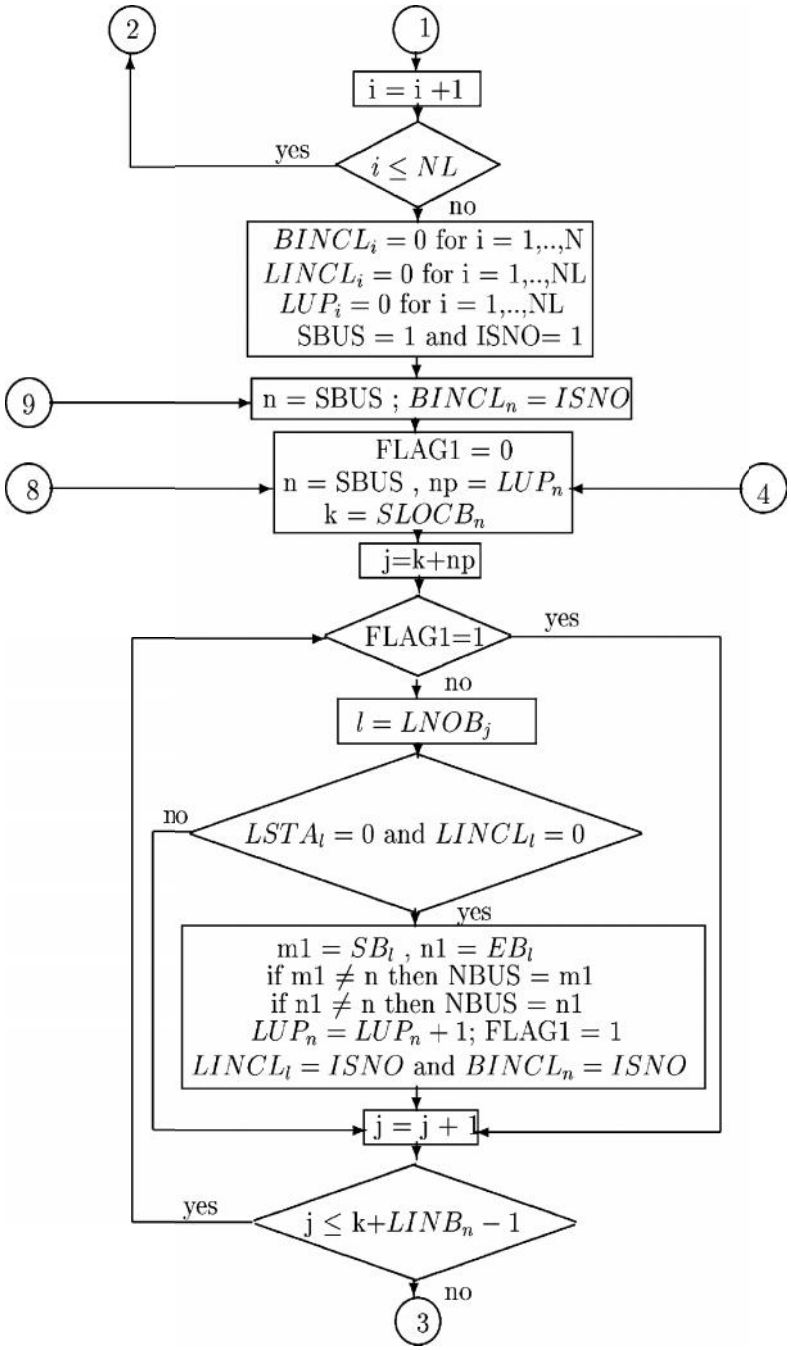

Fig.2. (continued)

4. INDICES FOR QUANTIFICATION OF LINE OUTAGE CONTINGENCY

The outage of lightly loaded lines in general will not appreciably affect the loading of other lines; only heavily loaded lines (say lines with flows greater than 60% of their MVA capacity) are selected for contingency analysis. Though, megavoltampere performance index, PI_{MVA} quantifies the extent of line overloads, but in our case over loaded remaining line(s) is also

removed for contingency analysis of a selected line. This may result in system islanding, loss of load and loss of generations. Therefore, voltage condition of the system has to be quantified to examine voltage stability condition of the system. For this purpose, voltage stability index is to be used to quantify stability condition of the system.

4.1. Megavoltampere due to line outage contingency index

The megavoltampere performance index, PI_{MVA} is used as an index for quantifying the extent of line overloads [1]. The performance index for line MVA is defined as

$$PI_{MVA} = \sum_{i=1}^{NO} \left[\frac{S_i \quad S_i^{\lim it}}{S_i^{\lim it}} \right]^2 \tag{4}$$

where

NO number of lines over loaded

S_i MVA flow in the over loaded line

S_i^{limit} MVA limit of the over loaded line.

4.2. Voltage stability index due to line outage contingency

It has been observed that voltage magnitudes, in general, do not give a good indication of proximity to voltage stability limit [8]. Therefore, indices are used to indicate proximity of voltage collapse quite effectively. The index used in this paper is as follows [9]

$$I_i = \frac{\mathrm{d}P_i / \mathrm{d}\delta_i}{\sum_{\substack{j=1 \\ j \neq i}}^{N} B_{ij} V_j} \tag{5}$$

where I_i is the voltage stability for ith bus. I_i for a bus decreases from 1.0 to its threshold 0.5 and if, I_i nears 0.5 voltage collapse in a power system is taken place. Therefore, bus with lowest value of I_i is the most critical bus as regards the voltage stability is concerned.

5. SOLUTION STEPS OF THE PROPOSED METHOD

The solution steps of the proposed algorithm are as follows:

Step 1. set k=1.

Step 2. Check whether;

if $S_k \leq L_f S^{limit}_k$ go to step 10:

where, L_f=fraction of the maximum line capacity.

Conduct load flow analysis applying appropriate modifications of [*B′*], [*B″*] and Y-bus matrices.

Step 3. Determine line flows in the remaining lines and in case of any over loading appearing in line(s) they are to be removed from network.

Step 4. Run topology processor to determine system network topology for line outage including islanding.

Step 5. Modify factored [*B′*] and [*B″*] matrices of the integrated system for the line which is disconnected from the system.

Step 6. Select slack bus for each island and the diagonal value of [*B′*] matrix corresponding to the each slack bus is replaced by 10^6. Similarly, for PV buses diagonal value of [*B″*] matrix corresponding to the each PV bus is replaced by 10^6. Carry out factorization of ordered [*B′*] and [*B″*] matrices.

Step 7. Compute generation from each generator in all the islands based on their inertia value at the time of system bifurcation using Eq. (2).

Step 8. Conduct a single piece fast decoupled load flow for the islanded system to determine the system state after system bifurcation, using the modified [*B′*] and [*B″*] matrices obtained in step (6). Compute PIMVA for that line outage checking the line flows for all other lines in the subsystems.

Step 9. Determine PI_{MVA} and Ii

Step 10. K=k+1

Step 11. Check whether k≤NL go to step (2).

Step 12. Stop

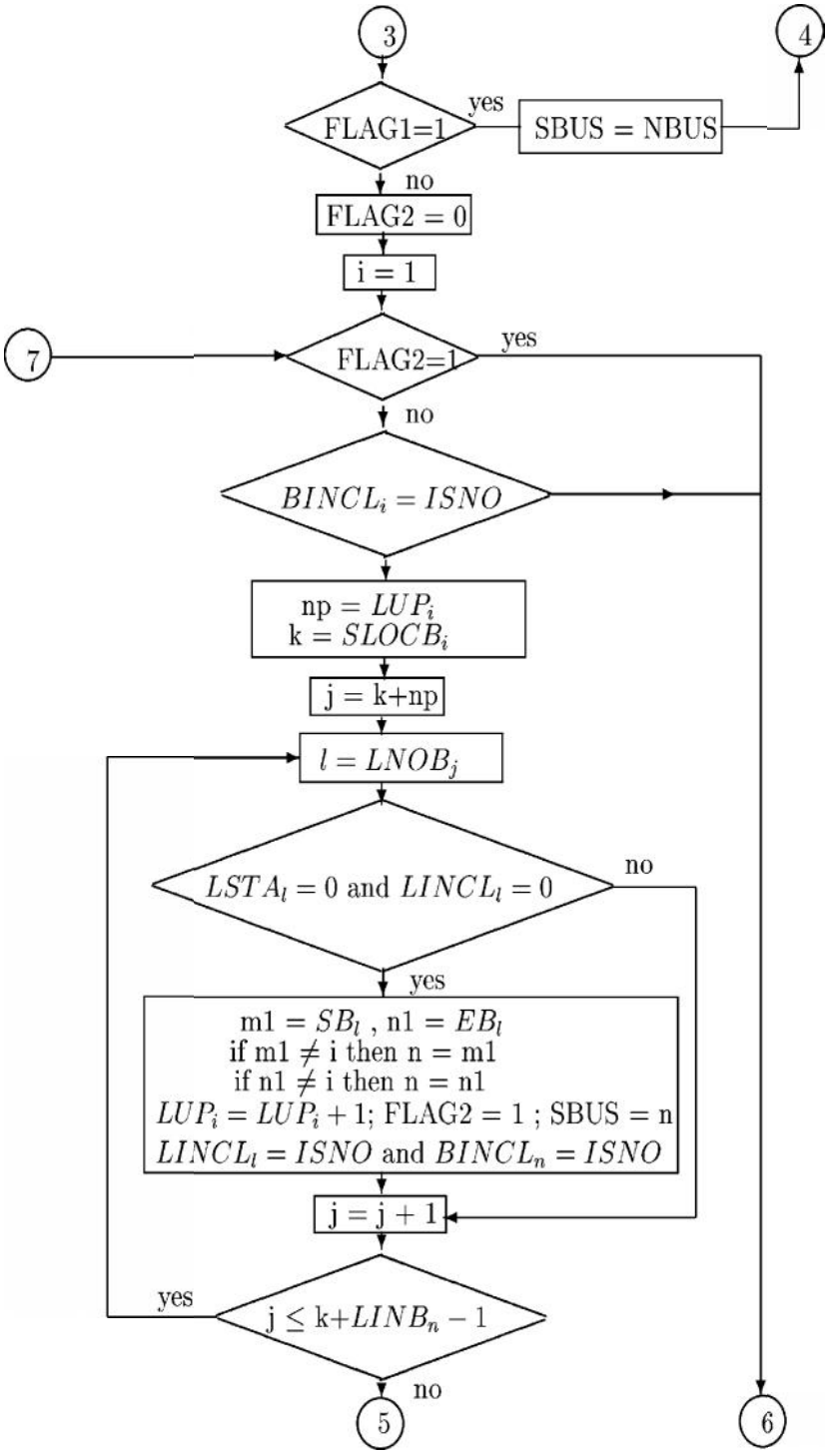

Fig.2. (continued)

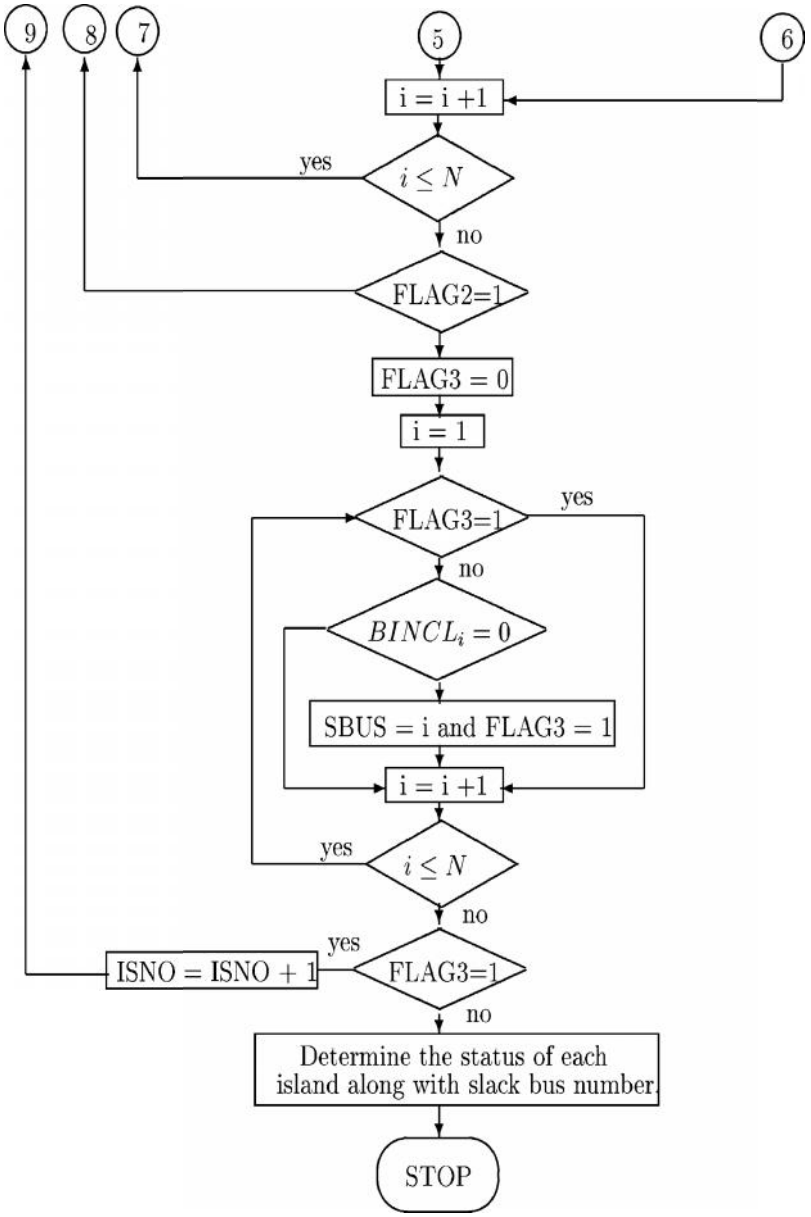

Fig.2. (continued)

6. SIMULATION RESULTS AND DISCUSSIONS

The proposed algorithm has been tested on IEEE 30BUS and IEEE 118 BUS systems. Table1 gives summary of the initial operating condition about the systems. The line outage contingency analysis is carried out for the lines having line flows more than 70% of their MVA capacity. For the selected contingency, line flows in remaining lines are determined using a load flow analysis. If line over load is detected on remaining line(s), this/these line(s) is/are removed and topology processor is used to determine system split and load flow

analysis is carried out for the modified network topology condition with generation rescheduling for the system as described in Section 2. Based on the system operating condition obtained from the load flow analysis, line over load index and voltage stability index are determined. These indices are determined for a few line outage contingency for lines having line flow above 70% of their capacity with line over load tolerance limits on line flow of over loaded lines with respect to their allowable capacity flow. Tables 2–5 represent line outage contingency results for a few lines having line flow above 70% of their capacity with line over load tolerance limits 100, 110, 120 and 125% for IEEE 30 bus system, respectively. Tables 6 and 7 represent line outage contingency results for a few lines having line flow above 70% of their capacity with line over load tolerance limits 100 and 110% for IEEE 118 bus system, respectively. It is observed from the simulation and analysis that use of different tolerance limits for the removal of over loaded lines due to a line outage contingency may play an important role in the operation of a power system. Effect of overloading tolerance limits on over loaded lines could have different effect for different line outage contingency analysis. For example, line outage contingency analysis of line connected between bus 12 and bus 15 for IEEE 30 bus system, with different overloading tolerance limits on over loaded lines indicate that if tolerance limits are set at 125% of their capacity flow, the voltage stability problem appears for this line outage up to tolerance limit of 120% could be avoided. Again, when no tolerance on line over load limits are allowed (i.e. allowing only 100% loading) load flow did not converge for three lines outage contingency analysis for IEEE 30 bus system, which is due to voltage stability problem for the changed network configuration of the system. Increase in tolerance limits to 110% reduces voltage instability problem to only one line outage contingency, i.e. line connected between bus 12 and bus 15. Similarly, in case of IEEE 118 bus system, when tolerance limit is changed from 100 to 110%, the line outage contingency situation for line between bus 89 and bus 92 shows different operational situations. With tolerance limit 100%, system islanding has occured and load flow analysis for the 2nd island did not converge. Increase in tolerance limit from 100 to 110% has avoided system islanding. Further, for different tolerance limits, system islanding situations are also different. The programwas run on a PCwith P-IVprocessor and LINUX operating

system. For all type of contingencies (i.e. with and without network split) same sparse ordered [*B′*] and [*B″*] matrices are modified according to the change in network topology. Therefore, sparse optimal ordering of both [*B′*] and [*B″*] matrices are done only at the beginning. Maximum CPU time required for contingency analysis for IEEE 30 bus system is observed as 20 ms when, three islands are created due to line outage contingency. Similarly, 70 ms CPU time is taken to execute line outage contingency analysis for IEEE 118 bus system.

Table 1. Summary of system status

System summary of IEEE 30 and 118 BUS systems

IEEE system	**Total buses**	**Total lines**	P_{GT}	P_{DT}	P_{L}
IEEE 30 bus	30	41	3.684075	3.588	0.096075
IEEE 118 bus	118	178	41.798551	40.392	1.406551

Table 2. Line outage contingency indices for few lines having line flow near to 70% of their capacity using criteria for removal of lines is 'remove lines if line flow>line capacity' for IEEE 30 bus system

Line outage connected between	Removed lines		PI_{MVA}	Ii	Island status	
	Connected between	%Over load			Information	Buses lines
10–21	12–15	30.669145	0.386	I_{22}=0.623	NIS=2	
	10–22	16.861031			IS_1=1	BI_1=29
	21–22	11.935315				LI_1=35
	6–9	0.306435			IS_2=0	BI_2=1
	4–12	2.320861				LI_2=0
15–18	19–20	32.239010	Nil	I_{30}=0.873	NIS=3	
	10–20	32.112228			IS_1=1	BI_1=27
	6–9	24.704755				LI_1=36
					IS2=0	BI_2=2
						LI_2=1
					IS_3=0	BI_3=1
						LI_2=0
19–20	12–15	98.181282	LFNC		NIS=3	
	15–18	74.339657			IS_1=1	BI_1=28
	18–19	15.646391				LI_1=34
	10–17	2.188753			IS_2=0	BI_2=1
	10–21	13.823487				LI_2=0
	4–12	30.212126			IS_3=0	BI_3=1
						LI_3=0
6–9	12–15	37.592367	0.995	I_{19}=0.795	NIS=1	
	4–12	26.982963			IS_1=1	BI_1=27
						LI_1=38
4–12	19–20	7.362055	LFNC		NIS=1	
	13.259030				IS_1=1	BI_1=27
	6–9	77.672066				LI_1=36
	28–27	3.302338				
12–15	12–14	22.478781	LFNC	NIS=2		
	19–20	6.039559			IS_1=1	BI_1=27
	10–20	1.949114				LI_1=36
	10–21	1.991911				BI_1=1
	6–9	23.719225				LI_1=0

Table 3. Line outage contingency indices for few lines having line flow near to 70% of their capacity using criteria for removal of lines is 'remove lines if line flow>1.1 line capacity' for IEEE 30 bus system

Line outage connected between	Removed lines		PIMVA	Ii	Island status	
	Connected between	%Over load			Information	Buses lines
10–21	12–15	30.669145	0.179	I_{22}=0.735	NIS=2	
	10–22	16.861031			IS_1=1	BI_1=29
	21–22	11.935315				LI_1=37
					IS_2=0	BI_2=1
15–18	19–20	32.239010	Nil	I_{30}=0.873	NIS=3	
	10–20	32.112228			IS_1=1	BI_1=27
	6–9	24.704755				LI_1=36
					IS_2=0	BI_2=2
						LI_2=1
					IS_3=0	BI_3=1
						LI_3=0
19–20	12–15	98.181282	0.409	I_{30}=0.857	NIS=3	
	15–18	74.339657			IS_1=1	BI_1=28
	18–19	15.646391				LI_1=35
	10–21	13.823487			IS_1=0	BI_2=1
	4–12	30.212126				LI_2=0
					IS_3=0	BI_3=0
						LI_3=0
6–9	12–15	37.592367	0.995	I_{19}=0.795	NIS=1	
	4–12	26.982963			IS_1=1	BI_1=27
						LI_1=38
4–12	10–17	13.259030	1.422	I_{17}=0.683	NIS=1	
	6–9	77.672066			IS_1=1	BL_1=30
						LI_1=38
12–15	12–14	22.478781	2.089	I_{14}=0.45	NIS=1	
	6–9	23.719225			IS_1=1	BL_1=30

Table 4. Line outage contingency indices for few lines having line having line flow near to 70% of their capacity using criteria for removal of lines is 'remove lines if line flow>1.2 line capacity' for IEEE 30 bus system

Line outage connected between	Removed lines		PIMVA	Ii	Island status	
	Connected between	%Over load			Information	Buses lines
10–21	12–15	30.669145	0.275	I_{15}=0.803	NIS=1	
					IS_1=1	BI_1=30
	21–22	11.935315				LI_1=39
15–18	19–20	32.239010	Nil	I_{30}=0.873	NIS=3	
	10–20	32.112228			IS_1=1	BI_1=27
	6–9	24.704755				LI_1=36
					IS_2=0	BI_2=2
						LI_2=1
					IS_3=0	BI_3=1
						LI_3=0
19–20	12–15	98.181282	0.409	I_{15}=0.837	NIS=2	
	15–18	74.339657			IS_1=1	BI_1=28
	4–12	30.212126				LI_1=36
					IS_2=0	BI_2=2
						LI_2=1
6–9	12–15	37.592367	0.995	I_{19}=0.795	NIS=1	
	4–12	26.982963			IS_1=1	BI_1=30
						LI_1=38
4–12	10–17	13.259030	1.422	I_{17}=0.683	NIS=1	
	6–9	77.672066			IS_1=1	BL_1=30
						LI_1=38
12–15	12–14	22.478781	2.089	I_{14}=0.45	NIS=1	
	6–9	23.719225			IS_1=1	BI_1=30
						LI_1=38

Table 5. Line outage contingency indices for lines connected between bus 15 and bus 18 and bus 12 and bus 15 using criteria for removal of lines is 'remove lines if line flow>1.25 times of line capacity' for IEEE 30 bus system

Line outage connected between	Removed lines		PIMVA	Ii	Island status	
	Connected between	% Over load			Information	Buses lines
15–18	19–20	32.239010	Nil	I_{30}=0.873	NIS=3	
	10–20	32.112228			IS_1=1	BI_1=27
						LI_1=37
					IS_2=0	BI_2=2
						LI_2=1
					IS_3=0	BI_3=1
						LI_3=0
					IS_1=1	BI_1=27
12–15			0.116	I_{19}=0.811	NIS=1	
					IS_1=1	BI_1=30
						LI_1=41

Table 6. Line outage contingency indices for few lines having line flow near to 70% of their capacity using criteria for removal of lines is 'remove lines if line flow>line capacity' for IEEE 118 bus system

Line outage connected between	Removed lines		PIMVA	Ii	Island status	
	Connected between	% Over load			Information	Buses lines
26–30	25–26	21.531483	0.011	I_{76}=0.889	NIS=2	
					IS_1=1	BI_1=117
						LI_1=177
					IS_2=0	BI_2=1
						LI_2=0
37–38	17–18	12.578149	0.571	I_{18}=0.793	NIS=1	
	17–30	4.173401			IS_1=1	BI_1=118
	12–66	2.035454				LI_1=175
89–92	82–83	0.126893	Nil	I_{23}=0.895	NIS=2	
	88–89	9.508981			IS_1=1	BI_1=110
	90–91	1.081410				LI_1=167
			LFNC		IS_2=1	BI_2=8
						LI_2=8

Table 7. Line outage contingency indices for few lines having line flow near to 70% of their capacity using criteria for removal of lines is 'remove lines if line flow>1.1 line capacity' for IEEE 118 bus system

Line outage connected between	Removed lines		PIMVA	Ii	Island status	
	Connected between	% Over load			Information	Buses lines
26–30	25–26	21.531483	0.011	I_{76}=0.889	NIS=2	
					IS_1=1	BI_1=117
						LI_1=177
					IS_2=0	BI_2=1
						LI_2=0
89–92	82–89	9.508981	0.388	I_{88}=0.737	NIS=1	
					IS_1=1	BI_1=118
						LI_1=177

7. CONCLUSION

The islanded systems are the subsystems of the main grid system, therefore, the optimally ordered sparse [*B′*] and [*B″*] matrices used for the load flow analysis of the grid system can be used for the islanded system applying proper modification with respect to change in network condition. The modification can be applied to the optimally ordered sparse [*B′*], [*B″*] and Y-bus matrices. Again, large values (10^6) are put in place of the diagonal elements corresponding to the slack buses of the islands in [*B′*] and [*B″*] matrices of the integrated system, which is already stored in ordered form. This reduces computational time to a considerable extent, which is evident for the CPU time taken for the execution of the proposed contingency analysis carried out for IEEE 30 and 118 bus systems. It is observed that line outage contingency analysis including the effect of tripping of over loaded line(s) due to the selected contingency with different tolerance limits provides different operating condition of the system. This information would constitute important criteria in the decision making in a power system planning, operation and control.

Appendix A

Let us six bus system shown in Fig. A1(a) bus 1 is taken as the slack for the integrated system.

Therefore, for the integrated six bus system [Δ P/V] and [δ] are related as follows:

$$\begin{bmatrix} \Delta P_1/\Delta V_1 \\ \Delta P_2/\Delta V_2 \\ \Delta P_3/\Delta V_3 \\ \Delta P_4/\Delta V_4 \\ \Delta P_5/\Delta V_5 \\ \Delta P_6/\Delta V_6 \end{bmatrix} = \begin{bmatrix} 10^6 & B'_{12} & B'_{13} & 0 & B'_{15} & 0 \\ B'_{21} & B'_{22} & B'_{23} & 0 & 0 & 0 \\ B'_{31} & B'_{32} & B'_{33} & B'_{34} & 0 & 0 \\ 0 & 0 & B'_{43} & B'_{44} & B'_{45} & 0 \\ B'_{51} & 0 & 0 & B'_{54} & B'_{55} & B'_{56} \\ 0 & 0 & 0 & 0 & B'_{65} & B'_{66} \end{bmatrix} \begin{bmatrix} \Delta\delta_1 \\ \Delta\delta_2 \\ \Delta\delta_3 \\ \Delta\delta_4 \\ \Delta\delta_5 \\ \Delta\delta_6 \end{bmatrix}$$

Let, the system get separated into two islands as shown in Fig. A1(b) and bus 1 and bus 4 as the slack buses for the two islands, respectively. As lines between 1–5 and 3–4 are disconnected, the modifications of B' elements of [B'] matrix are to be carried out as follows:

$B'_{15}=B'_{51}=0$, $B'_{55}=B'_{55}-B'_{15}$

$B'_{34}=B'_{43}=0$, $B'_{33}=B'_{33}-B'_{34}$, $B'_{44}=10^6$

$$\begin{bmatrix} \Delta P_1/\Delta V_1 \\ \Delta P_2/\Delta V_2 \\ \Delta P_3/\Delta V_3 \\ \Delta P_4/\Delta V_4 \\ \Delta P_5/\Delta V_5 \\ \Delta P_6/\Delta V_6 \end{bmatrix} = \begin{bmatrix} 10^6 & B'_{12} & B'_{13} & 0 & 0 & 0 \\ B'_{21} & B'_{22} & B'_{23} & 0 & 0 & 0 \\ 0 & B'_{32} & B'_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & 10^6 & B'_{45} & 0 \\ 0 & 0 & 0 & B'_{54} & B'_{55} & B'_{56} \\ 0 & 0 & 0 & 0 & B'_{65} & B'_{66} \end{bmatrix} \begin{bmatrix} \Delta\delta_1 \\ \Delta\delta_2 \\ \Delta\delta_3 \\ \Delta\delta_4 \\ \Delta\delta_5 \\ \Delta\delta_6 \end{bmatrix}$$

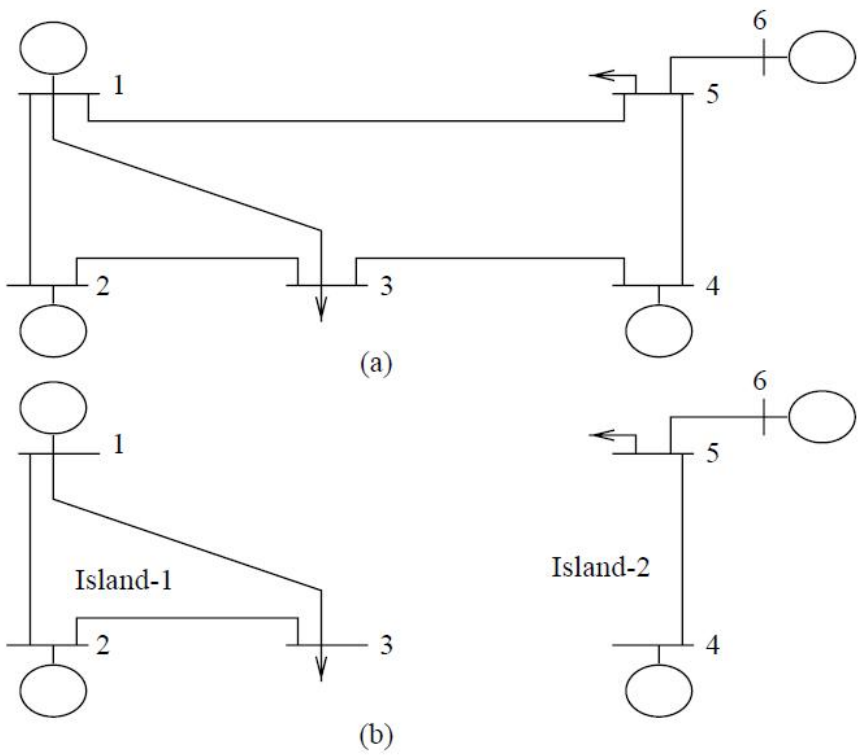

Fig.A1. Sample 6 bus system (a) before system bifurcation and (b) after bifurcation into two islands

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